WHAT IS CLAIMED IS:

1. A variable gain amplifier comprising a differential input amplifier which includes transistors T1 and T2 that constitute a differential pair, and a constant current circuit Is that operates as an absorption current circuit for the transistors T1 and T2 constituting the differential pair, and a variable impedance which is connected between sources of the respective transistors T1 and T2 of said differential input amplifier, wherein a gain of said differential input amplifier is made variable by variably controlling a value of said variable impedance.

2. A variable gain amplifier according to claim 1, wherein said transistors T1 and T2 constituting said differential pair have their gates respectively connected to differential inputs Vi^+ and Vi^- and have their drains respectively connected to ends of load resistances RL1 and RL2 being respectively connected to a supply voltage VDD at their other ends, drain - source paths of transistors T3 and T4 which serve as said variable impedance are respectively inserted and connected between the sources of said respective transistors T1 and T2 and the constant current circuit Is, and a gain control voltage Vgc is connected to gates of the transistors T3 and T4, whereby the gain of said differential input amplifier is variably controlled by controlling the value

of said variable impedance.

3. A variable gain amplifier according to claim 1, wherein the constant current circuit Is includes a first constant current circuit Is1 and a second constant current circuit Is2, said transistors T1 and T2 constituting said differential pair have their gates respectively connected to differential inputs Vi^+ and Vi^-, have their drains respectively connected to ends of load resistances RL1 and RL2 being respectively connected to a supply voltage VDD at their other ends and have their sources respectively connected to the first and second constant current circuits Is1 and Is2, drain - source paths of transistors T3 and T4 which serve as said variable impedance are connected between the sources of said respective transistors T1 and T2, and a gain control voltage Vgc is connected to gates of the transistors T3 and T4, whereby the gain of said differential input amplifier is variably controlled by controlling the value of said variable impedance.

4. A variable gain amplifier according to claim 2, further comprising a resistance Rs which determines a minimum gain of said differential input amplifier, and which is connected between said sources of said transistors T1 and T2.

5. An AM-modulated signal reception circuit which receives

an AM-modulated signal Vi in two states of a large amplitude state and a small amplitude state, and which identifies the two states; comprising:

a gain control amplifier block (GCA-B) whose gain is controlled by a peak value voltage Vp from a peak value input terminal, and which amplifies the input AM-modulated signal Vi so as to deliver an output Vo;

an envelope detection circuit (SDet) which detects an envelope of the amplification output Vo of said gain control amplifier block (GCA-B);

a comparator circuit (Comp) which compares an output of said envelope detection circuit (SDet) and a reference voltage VR2 so as to output a logic signal TCO; and

a peak detection circuit (PDet) which receives the output signal TCO of said comparator circuit (Comp) as a control input, which, when the control input is an "H" status (or "L" status), detects a peak value of the output Vo of said gain control amplifier block (GCA-B) so as to deliver the detection peak value Vp to the peak value input terminal of said control amplifier block (GCA-B), and which, when the output signal of said comparator circuit (Comp) has changed into the "L" status (or "H" status), holds the detection peak value Vp detected immediately before the change, so as to output the held detection peak value to said peak value input terminal.

6. An AM-modulated signal reception circuit according to claim 5, wherein said peak detection circuit (PDet) includes:

a rectification circuit (Rec1) which rectifies the output signal Vo of said gain control amplifier block (GCA-B);

a resistance R1 for a discharge path, which is connected between an output of said rectification circuit (Rec1) and ground (or a supply voltage);

a transfer gate (TG1) whose conduction terminal is connected to the output of said rectification circuit (Rec1) at its one end and is connected to said peak value input terminal of said gain control amplifier block (GCA-B) at its other end, which receives said output signal TCO of said comparator circuit (Comp) as a control input, and which falls into a conductive state when the control input is in said "H" status (or "L" status) and falls into a nonconductive state when said control input is in said "L" status (or "H" status); and

a peak holding capacitance C1 which is connected between the other end of the conduction terminal of said transfer gate (TG1) and ground (or a supply voltage).

7. An AM-modulated signal reception circuit according to claim 5, wherein said peak detection circuit (PDet) includes:

a rectification circuit (Rec1) which rectifies the output signal Vo of said gain control amplifier block (GCA-B);

a peak holding capacitance C1 which is connected between

an output of said rectification circuit (Rec1) and ground (or a supply voltage);

a resistance R1 for a discharge path, one end of which is connected to the output of said rectification circuit (Rec1) and said peak value input terminal of said gain control amplifier block (GCA-B); and

a transfer gate (TG1) whose conduction terminal is connected to the other end of said resistance R1 for the discharge path at its one end and is connected to the ground at its other end, which receives said output signal TCO of said comparator circuit (Comp) as a control input, and which falls into a conductive state when the control input is in said "H" status (or "L" status) and falls into a nonconductive state when said control input is in said "L" status (or "H" status).

8. An AM-modulated signal reception circuit according to claim 5, wherein said peak detection circuit (PDet) includes:

a rectification circuit (Rec1) which rectifies the output signal Vo of said gain control amplifier block (GCA-B);

a peak holding capacitance C1 which is connected between an output of said rectification circuit (Rec1) and ground (or a supply voltage); and

a constant current circuit I1 for a discharge path and provided with a control input, whose current output terminal is connected to the output of said rectification circuit (Rec1)

and said peak value input terminal of said gain control amplifier block (GCA-B), whose ground terminal is connected to ground, which receives said output signal TCO of said comparator circuit (Comp) as the control input, and which outputs a constant current I1 from the current output terminal when said control input is in said "H" status (or "L" status) and turns OFF the constant current I1 when said control input is in said "L" status (or "H" status).

9. An AM-modulated signal reception circuit according to claim 6, wherein said peak detection circuit (PDet) further includes a second discharge path (resistance R3 or constant current circuit I3) through which a current smaller than that of said resistance R1 for the discharge path or said constant current circuit I1 for the discharge path is caused to flow, and which is connected in parallel with said peak holding capacitance C1.

10. An AM-modulated signal reception circuit according to claim 6, wherein said transfer gate (TG1) or said constant current circuit I1 for the discharge path and provided with the control input as is included in said peak detection circuit (PDet) is controlled by a signal which is obtained by OR synthesis between said output signal TCO of said comparator circuit (Comp) and an external control signal HS-AGC.

11. An AM-modulated signal reception circuit according to claim 6, further comprising forcible discharge means for forcibly discharging charges stored in said peak holding capacitance C1 of said peak detection circuit (PDet), by an external control signal RESET.

12. An AM-modulated signal reception circuit according to claim 6, further comprising control means for forcibly turning ON said transfer gate TG1 as is included in said peak detection circuit (PDet), in a case where said output signal TCO of said comparator circuit (Comp) does not fall into the output status corresponding to the large amplitude input, for a predetermined time period.

13. An AM-modulated signal reception circuit according to claim 12, wherein said control means for the forcible turn-ON includes a timer circuit which receives said output signal TCO of said comparator circuit (Comp) as an input, and which outputs "0" as soon as said output signal TCO has changed into the output status corresponding to the large amplitude reception mode and outputs "1" upon lapse of a predetermined time period when said output signal TCO has changed into the output status corresponding to the small amplitude reception mode, and OR synthesis means for executing OR synthesis between the output

of said timer circuit and said output signal TCO of said comparator circuit (Comp) and then outputting a signal for the control.

14. An AM-modulated signal reception circuit according to claim 6, further comprising means for forcibly turning OFF charge and discharge of said peak holding capacitance C1 of said peak detection circuit (PDet).

15. An AM-modulated signal reception circuit according to claim 6, further comprising a delay circuit (D) which delays the output signal TCO of said comparator circuit (Comp), a monostable multivibrator (MM) which receives an output of said delay circuit (D) so as to output a pulse of predetermined time width, and a changeover switch (S) which changes-over the output of said monostable multivibrator (MM) and said output signal TCO of said comparator circuit (Comp) so as to feed the changed-over output to the control input terminal of said transfer gate TG1 (or constant current circuit I1 capable of turn ON/OFF) of said peak detection circuit (PDet).

16. An AM-modulated signal reception circuit according to claim 6, further comprising a delay circuit (D) which delays the output signal TCO of said comparator circuit (Comp), a monostable multivibrator (MM) which receives an output of said delay circuit D so as to output a pulse of predetermined time

width, an AND circuit which executes AND synthesis between the output of said monostable multivibrator (MM) and said output signal TCO of said comparator circuit (Comp), and a changeover switch (S) which changes-over an output of said AND circuit and said output signal TCO of said comparator circuit (Comp) so as to feed the changed-over output to the control input terminal of said transfer gate TG1 (or constant current circuit I1 capable of turn ON/OFF) of said peak detection circuit (PDet).

17. An AM-modulated signal reception circuit which simultaneously receives radio waves from a plurality of stations, comprising:

a first tuning circuit which includes an antenna coil L1 and a tuning capacitance C1 for tuning reception of the radio wave of carrier frequency f1;

a preamplifier (PA1) which amplifies an output signal of said first tuning circuit;

a second tuning circuit which includes an antenna coil L2 and a tuning capacitance C2 for tuning reception of the radio wave of carrier frequency f2;

a preamplifier (PA2) which amplifies an output signal of said second tuning circuit;

an adder circuit (Add) which adds up outputs of the preamplifiers (PA1) and (PA2);

a gain control amplifier block (GCA-B) which amplifies

an output signal Vi of said adder circuit (Add) by lowering its gain when a DC control voltage Vp rises and by heightening its gain when the DC control voltage Vp lowers, and which includes two band-pass filters (BPF1, BPF2) that output a band signal Vo1 having a bandwidth $\Delta f1$ at the center frequency f1 and a band signal Vo2 having a bandwidth $\Delta f2$ at the center frequency f2;

a peak detection circuit (PDet) which includes a peak holding capacitor C1, a rectification circuit (Rec1a) that rectifies the band signal Vo1 so as to charge said peak holding capacitor C1, a rectification circuit (Rec1b) that rectifies the band signal Vo2 so as to charge said peak holding capacitor C1, and a discharge resistance R1 that discharges stored charges of said peak holding capacitor C1, and which outputs a charged voltage of said holding capacitor C1 as the control voltage Vp to said gain control amplifier block (GCA-B);

an envelope detection circuit (SDet) which includes a peak holding capacitor C2, a rectification circuit (Rec2a) that rectifies said band signal Vo1 so as to charge said peak holding capacitor C2, a rectification circuit (Rec2b) that rectifies said band signal Vo2 so as to charge said peak holding capacitor C2, and a discharge resistance R2 that discharges stored charges of said peak holding capacitor C2, and which outputs a charged voltage of said peak holding capacitor C2 as an envelope detection output; and

a comparator (Comp) which compares the output of said

envelope detection circuit (SDet) and a reference voltage VR2 so as to output a signal TCO.

18. An AM-modulated signal reception circuit according to claim 17, further comprising a second adder circuit (Add2) which adds up the output of the band-pass filter (BPF1) of said gain control amplifier block (GCA-B), for extracting said band signal Vo1 having the bandwidth $\Delta f1$ at said center frequency f1, and the output of the band-pass filter (BPF2) thereof for extracting said band signal Vo2 having the bandwidth $\Delta f2$ at said center frequency f2, and an output of which is inputted to said peak detection circuit (PDet) and said envelope detection circuit (SDet).

19. An AM-modulated signal reception circuit according to claim 17, wherein the antenna coils L1 and L2 are bar antennae, which are arranged on a horizontal plane so as to be orthogonal to each other, a tuning frequency of said antenna coil L1 and said tuning capacitance C1 and a tuning frequency of said antenna coil L2 and said tuning capacitance C2 are set at an identical frequency f, a phase changeover switch (S) which changes-over an output phase of said preamplifier (PA2) between positive and negative phases is inserted between the output of said preamplifier (PA2) and an input terminal of said adder circuit (Add), and the band-pass filters built in said gain control

amplifier block (GCA-B) are constructed as a single band-pass filter (BPF).

20. An AM-modulated signal reception circuit according to claim 18, wherein:

the antenna coils L1 and L2 are bar antennae, which are arranged on a horizontal plane so as to be orthogonal to each other, and a tuning frequency of said antenna coil L1 and said tuning capacitance C1 and a tuning frequency of said antenna coil L2 and said tuning capacitance C2 are set at an identical frequency f1;

a tuning capacitance C3 which can be electrically connected and disconnected by a switch (S1) is added to said tuning capacitance C1, while a tuning capacitance C4 which can be electrically connected and disconnected by a switch (S2) is added to said tuning capacitance C2;

a tuning frequency of said antenna coil L1 and the tuning capacitances C1 and C3, and a tuning frequency of said antenna coil L2 and the tuning capacitances C2 and C4 are set at an identical frequency f2; and

a phase changeover switch (S) which changes-over an output phase of said preamplifier (PA2) between positive and negative phases is inserted between the output of said preamplifier (PA2) and an input terminal of said adder circuit (Add).

21. A reception circuit having a differential input type preamplifier (PA) in which an antenna coil L is connected across differential input terminals, comprising a center tap which is mounted on the antenna coil L so as to feed an input bias of the differential input type preamplifier (PA) from said center tap.

22. A detection circuit in an AM-modulated signal reception circuit which receives an AM-modulated signal Vi in two states of a large amplitude state and a small amplitude state, and which identifies the two states; comprising:

a timing extraction unit which extracts a carrier frequency component from an output signal Vo of an AGC circuit that controls and amplifies the received AM-modulated signal to a predetermined amplitude value, and which outputs a clock pulse CL that is timed to a peak position of an amplitude of an output signal Vo of the AGC circuit;

a clock generation unit to which the clock pulse CL is inputted so as to output a sampling clock pulse SCL timed to the peak position;

a reference voltage setting unit which outputs a comparison reference voltage VR2; and

a sampling comparison-and-holding unit which samples and compares the output Vo of said AGC circuit and the comparison reference voltage VR2 so as to output a comparison result signal

TCO when the sampling clock pulse SCL is inputted, and which holds the sampled and compared voltages until the next sampling clock pulse SCL is inputted.

23. A detection circuit according to claim 22, wherein said reference voltage setting unit is a voltage division circuit which outputs the reference voltage value VR2 that is obtained by dividing an output signal Vp of a peak detection circuit (PDet) included in said AGC circuit.

24. A detection circuit according to claim 22, wherein said timing extraction unit includes a limit amplifier (LIM) which limit-amplifies the output Vo of said AGC circuit, and a first monostable multivibrator (MM1) which outputs the clock pulse CL when triggered by an output of said limit amplifier (LIM).

25. A detection circuit according to claim 22, wherein said timing extraction unit includes a first phase shift circuit (PS1) which advances (or retards) a phase of the output signal Vo of said AGC circuit so as to deliver an output Vo1, a second phase shift circuit (PS2) which retards (or advances) the phase of said output signal Vo of said AGC circuit so as to output the resulting signal, and a limit amplifier (LIM) which limit-amplifies the output of said second phase shift circuit

(PS2) so as to output the clock pulse CL.

26. A detection circuit according to claim 22, wherein said clock generation unit is a second monostable multivibrator (MM2) which receives the clock pulse CL so as to generate the sampling clock pulse SCL.

27. A detection circuit according to claim 22, wherein said clock generation unit includes a delay circuit (Dt) which inverts and delays the clock pulse CL, and a logic synthesis circuit (NOR/AND) which executes NOR or AND synthesis between an output of said delay circuit (Dt) and said clock pulse CL so as to output the sampling clock pulse SCL.

28. A detection circuit according to claim 22, wherein said sampling comparison-and-holding unit includes a holding capacitance C one end of which is grounded, a transfer gate (TG) which brings a path between the output Vo of said AGC circuit and the other end of said holding capacitance C, into a conductive state when the sampling clock pulse SCL is inputted, and a comparator (Comp) which compares a voltage at said other end of said holding capacitance C and the comparison reference voltage VR2.

29. A detection circuit according to claim 25, wherein

said sampling comparison-and-holding unit includes a hysteresis type comparator (Comp) whose output signal TCO is determined in accordance with differential inputs, and which holds a logic output status assumed immediately before opening, in an input open state, and a transfer gate (TG) which, when the sampling clock pulse SCL is inputted, falls into a conductive state so as to connect the output Vo1 of said first phase shift circuit (PS1) and the reference voltage VR2 to the differential inputs of said hysteresis type comparator (Comp).

30. A detection circuit according to claim 25, wherein said sampling comparison-and-holding unit includes a comparator (Comp) which compares the output signal Vo1 of said first phase shift circuit (PS1) and the reference voltage VR2, and a D-type flip-flop which receives an output of said comparator (Comp) as its data input D, which receives the sampling clock pulse SCL as its clock input CK, and which delivers its logic output Q as the logic output TCO of the AM-modulated signal detection circuit.

31. A detection circuit according to claim 28, wherein said sampling comparison-and-holding unit further includes a resistance R which is inserted into a contact point between said transfer gate (TG) and said holding capacitance C.

32. A detection circuit according to claim 30, wherein said D-type flip-flop of said sampling comparison-and-holding unit includes a serial-in parallel-out shift register (SHR) of n bits (n being an odd number) which receives an output of said comparator (Comp) as its data input D and also receives the sampling clock pulse SCL as its clock input CK, and a majority circuit which subjects "H"/"L" outputs of parallel outputs Q1 - Qn of said shift register (SHR) to majority processing, so as to output "H" when the number of bits of the "H" outputs is larger and to output "L" when smaller.

33. A detection circuit according to claim 25, wherein said timing extraction unit further includes a tank tuning circuit which is interposed between said second phase shift circuit (PS2) and said limit amplifier (LIM).